GPS2VME: User's Guide

The GPS2VME interface is a standard VME slave module which converts standard time telegrams from a Truetime XL-DC GPS receiver into a binary format (major time). An internal counter counts the 10 MHz pulses also supplied from the XL-DC via a separate cable (minor time with a resolution of 100ns). The third timing input to the GPS2VME is a 1PPS (pulse per second) that resets the 10 MHz counter. An active trigger input causes a AMANDA specific time record to be written into the internal FIFO. These time records are read out over the VME bus. The module also provides some additional functions like a programmable pulser and a calibration output.

History

Actually there are 3 different GPS modules with VME interface in MAPO.

1. "GPSAMD" – a module which is very similar in its structure to the "GRS2" Camac interface module. It incorporates a Siemens C515C microcontroller and a Lattice programmable device.
   This module has been used in the μ-DAQ and the Supernova system. It has been replaced in summer 2003 by the newer "GPS2VME" modules. Do not use it anymore!

2. "GPS2VME" – this is a newer version of "GPSAMD" with extended functionality.
   It is based on an ALTERA programmable device, which implements as well as an internal processor as the VME interface logic.
   Due to different design requirements (μ-DAQ, Supernova and since 2003 TWR and VLF-veto) this modul exists in 2 firmware versions, but with identical control program. This new module contain a special ID-register, which can be read out via the VME interface. Two different ID's are used to distinguish between the two firmware versions.

VME – Interface:

- All accesses must be performed using 32 bit addresses with address modifier
  AM = 0x09 (FIFO and register access) or
  AM = 0x0f (FIFO access in Block Transfer Mode)

- VME /D16 and VME /D32 are allowed (FIFO access only with VME /D32)

Board base address:

VME A31 … A24, selectable by means of 2 hex rotary switches:

Switch 1 corresponds to A31 … A28;
Switch 2 corresponds to A27 … A24

Base + 0x0: **Control/ Status Register,** read/ write

Bit	Write Function	Read Function	Value after Reset	Note
0	Local Reset	No read back!	0	1)
1	Source of Year	` Source of Year`-Bit	0	2)
2	-	GPS 10MHz Clock Status	0	3)
3	Enable Pulser	'Enable Pulser' Bit	0	1)
4	-	FIFO not empty flag	0	4)
5	-	FIFO full flag	0	4)

1) For Local Reset and Pulser:
Bit = 0 → off
Bit = 1 → on (Reset aktiv or Pulser enable)

2) Bit = 1 → "Year" information from GPS TRUE Time XL time telegram
Bit = 0 → "Year" information from VME register
Please note: the year information is only requested from the XL-DC if this bit is changing from 0 → 1

3) Bit = 0 → GPS status not o.k.
Bit = 1 → GPS status o.k.

4) Bit 4 = 0 → FIFO empty
Bit 4 = 1 → FIFO **n o t** empty
Bit 5 = 0 → FIFO **n o t** full
Bit 5 = 1 → FIFO full

Base + 0x4: **Frequency Divider Register for the Calibration Pulse Output,** write only

Bit	Write Function	Read Function
11 … 0	Frequency Divider Register	-

The pulser output must be enabled by writing a '1' to the 'Pulser Enable' bit in the Control Register. The Frequency Divider Register controls the period of the pulser output. Writing a '0' disables the pulser. Writing a '1'sets a 1 ms period, a value of '4095' corresponds to 4095 ms.

Base + 0x8: **"Year"-Register,** read/write only

Bit	Write Function	Read Function
7 … 0	"Year" (2 hex digits)	Actual "Year" setting

The "Year"- value in the Event Data Block can be taken from either the GPS time telegram (which needs to send out a request to the True Time XL device, see above) or the above register which can be set by a VME write.

Base + 0xC: **ID/Led-Register** read/write

Bit	Write Function	Read Function
15 … 0	-	Module ID
2 … 0	Switch on VME-leds	-

Write function (bit 2…0): writing a "1" to the corresponding bits will switch on the front panel leds *VME2.. VME0*

Read Function: read the module ID (fixed value!):

Bit	15 … 12	11 … 8	7 ... 4	3 … 0
	a or b	Firmware release	Altera release	Board release

Please, note: Two different board releases are in use:

Module ID = **b232** → this board can be used in µ-DAQ, TWR.
This board can write different types of time records into the FIFO and also provides the VLF veto function
Module ID = **a221** → No VLF veto and a fixed time record format! This board is for use in Supernova systems

Base + 0x10: **FIFO Data out.**

Port is read only! A write to that address will cause a bus error!

Event Data Block Structure in FIFO:

Word #	Bit	Content
1	23 … 00	10 MHz Frequency Count
2	23 … 00	GPS time Telegram #1
3	23 … 00	GPS time telegram #2
4	23 … 22 21 … 00	Event Tag Event Counter

Format of GPS time word #1:
Bit: 23 … 00

Second's Count starting at 00:00:00 of the actual year
(low order 24 bit)

Format of GPS time word #2:

Bit:	23 … 20	19 … 16	15 … 08	07 … 00
	Status	TQC	Year (2 hex digits)	Second's Count (high order 8 bit)

where: TQC - True Time Quality Character as received via the RS-232 input from the GPS.
The Order of quality is:
0 (best), E, A, 3 and F (worst).

To set the actual year value a special time telegram must be sent out by the GPS!

Status – GPS Clock status:

Bit 20 (LSB)	1 PPS Bit: is high if 1 PPS signal has been present
Bit 21	10 MHz: is high if 10 MHz has been stable
Bit 22	COM Bit: is high if SIO input has been valid and incrementing
Bit 23 (MSB)	TIME Bit : is high if SIO input has matched internal time

Note: GPSOK-led is on if status = '1111'

Event Counter

The number of events (i.e. the number of pulses at the TRIG-inputs) after the last `Local Reset`.

Event Tag

'00' - for normal events
'11' - for Tag events (used in TWR-readout)

Please note:

Trigger inputs are:
a221-modules → the front panel NIM or the ECLin inputs
b232-modules → the front panel NIM or the backplane ECLin inputs

A Tag event will be written into the FIFO on an active signal at the front ECLin input (b232-modules only!)

Base + 0x14: **VLF control word 1**

Bit	23 … 16	15 ... 8	7 … 0
Write	VLF_on3	VLF_on2	VLF_on1
Read	VLF_on3	VLF_on2	VLF_on1

Base + 0x18: **VLF control word 2**

Bit	23 … 16	15 ... 8	7 … 0
Write	Overlap	Duration	VLF_on4
Read	Overlap	Duration	VLF_on4

Please note: VLF_on1 … VLF_on4 are specified in minutes, duration and overlap in seconds!

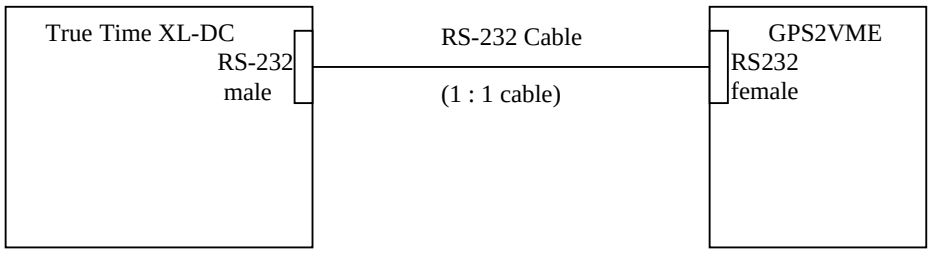
Base + 0x1C: **VLF control Register** write only

Bit	Write Function	Read Function
0	Bit = 0 → VLF enabled Bit = 1 → VLF disabled	-

→ *After reset VLFveto is enabled!*

GPS – Interface

GPS Connection to GPSAMD:



Pin-Assignments

RS-232 Connector (Front panel Host and GPS connectors):

Pin	Signal	Comment
1	nc	
2	Tx Data	
3	Rx Data	
4	nc	
5	GND	
6 .. 9	nc	

Front Panel ECL input, Pulser and Calibration Outputs:

Pin	Signal	Pin	Signal	Front Panel Label
1	Pulse Out +	2	Pulse Out -	'POut'
3	1 PPS Out +	4	1 PPS Out -	'CalOut'
5	F ECL In +	6	F ECL In -	'ECLin'
7	nc	8	nc	
9	GND	10	GND	'GND'

ECLinput from the Rear connector P2:

Pin Row A	Signal	Pin Row C	Signal
…		…	
11	R ECL In +	11	R ECL In -
…		…	

Lemo-Connector: PPS1

Pin	Signal	Comment
1	1 PPS In	TTL-Input >= 110ns

Please note: this input is terminated on board with 50 Ohms!

Lemo-Connector: 10 MHz

Pin	Signal	Comment
1	MHz 10 In	TTL (or Sine) -Input 10 MHz

Please note: this input is terminated on board with 50 Ohms!

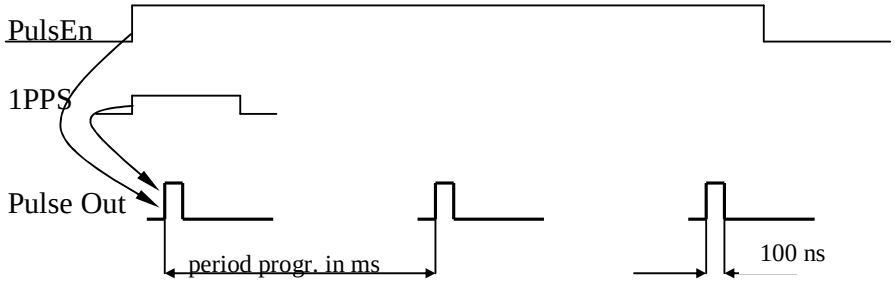
LEMO-Connector: TRIG

Pin	Signal	Comment
1	NIM-TRIG-In	NIM-Input >= 10 ns

Please note: this input is terminated on board with 1KOhm to allow daisy chaining of more than one module. The last module in a chain (or the only one) must terminate the trigger input with 50 Ohms!

Pulser Output (labeled 'POut' on the front panel):

Differential ECL signal; pulse width 100 ns, period programmable from 1 to 4096 ms by writing to the Frequency Divider Register

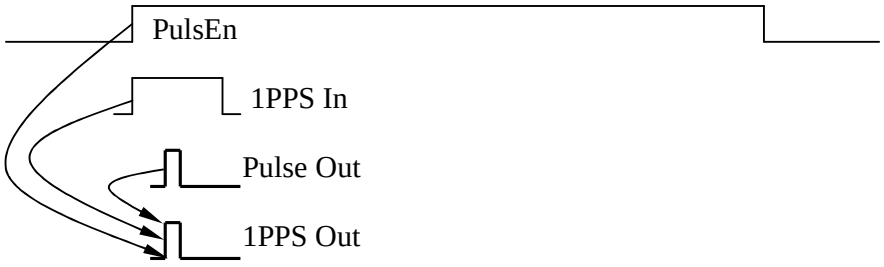


VLFveto Output (labeled 'CalOut' on the front panel, b232-modules only):

VLFveto output, differential ECL signal

1PPS Output (labeled 'CalOut' on the front panel, a221-modules only):

Differential ECL signal; pulse width is 100 ns, period is 1 second.



Please note: the pulse sequences at CalOut and POut are synchronized to the 1 PPS and the 10 MHz inputs from the GPS

LED Signals:

TRIG-Led:	on when a trigger input is processed
PULSE-Led:	blinking when the pulser is active
GPSERR-Led:	on if one of the bits of the GPS status is false
GPSOK-Led:	on if the GPS status is'1111'
VME3-Led:	on if the VLF veto signal is on

VME Access Status Led's: Iack, AS, DS0, Write, Dtack, Lword

Led's, programmable via VME-Bus: VME0 ..VME2
Led's, programmable via board internal NIOS processor: NIOS0 .. NIOS3

NIOS0 on → NIOS processor is running the control program
NIOS1 on → time telegram from XL-DC received